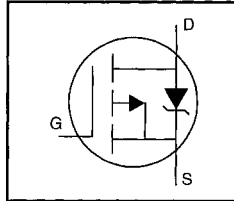


### HEXFET® Power MOSFET

- Isolated Package
- High Voltage Isolation= 2.5KVRMS ⑤
- Sink to Lead Creepage Dist.= 4.8mm
- P-Channel
- 175°C Operating Temperature
- Dynamic dv/dt Rating
- Low Thermal Resistance



$$V_{DSS} = -100V$$

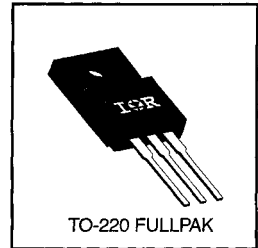
$$R_{DS(on)} = 0.30\Omega$$

$$I_D = -7.7A$$

### Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



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
### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10 V$	-7.7	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ -10 V$	-5.4	
$I_{DM}$	Pulsed Drain Current ①	-31	
$P_D @ T_C = 25^\circ C$	Power Dissipation	42	W
	Linear Derating Factor	0.28	W/°C
$V_{GS}$	Gate-to-Source Voltage	±20	V
$E_{AS}$	Single Pulse Avalanche Energy ②	380	mJ
$I_{AR}$	Avalanche Current ①	-7.7	A
$E_{AR}$	Repetitive Avalanche Energy ①	4.2	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.5	V/ns
$T_J$	Operating Junction and	-55 to +175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	


### Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	3.6	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	—	65	

**Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

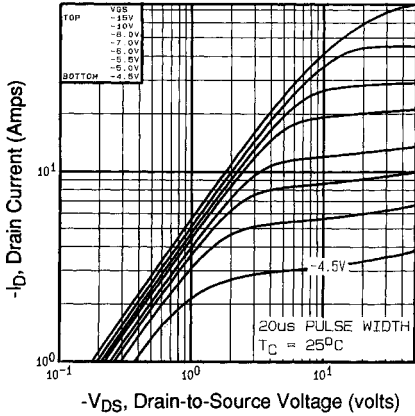
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	-100	—	—	V	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA
ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub>	Breakdown Voltage Temp. Coefficient	—	-0.10	—	V/°C	Reference to 25°C, I <sub>D</sub> =-1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	0.30	Ω	V <sub>GS</sub> =-10V, I <sub>D</sub> =-4.6A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	-2.0	—	-4.0	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA
g <sub>fs</sub>	Forward Transconductance	3.4	—	—	S	V <sub>DS</sub> =-50V, I <sub>D</sub> =-4.6A ④
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	-100	μA	V <sub>DS</sub> =-100V, V <sub>GS</sub> =0V
		—	—	-500		V <sub>DS</sub> =-80V, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	-100	nA	V <sub>GS</sub> =-20V
	Gate-to-Source Reverse Leakage	—	—	100		V <sub>GS</sub> =20V
Q <sub>g</sub>	Total Gate Charge	—	—	38	nC	I <sub>D</sub> =-12A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	6.8		V <sub>DS</sub> =-80V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	21		V <sub>GS</sub> =-10V See Fig. 6 and 13 ④
t <sub>d(on)</sub>	Turn-On Delay Time	—	12	—	ns	V <sub>DD</sub> =-50V
t <sub>r</sub>	Rise Time	—	52	—		I <sub>D</sub> =-12A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	31	—		R <sub>G</sub> =12Ω
t <sub>f</sub>	Fall Time	—	39	—		R <sub>D</sub> =3.9Ω See Figure 10 ④
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	860	—	pF	V <sub>GS</sub> =0V
C <sub>oss</sub>	Output Capacitance	—	340	—		V <sub>DS</sub> =-25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	93	—		f=1.0MHz See Figure 5
C	Drain to Sink Capacitance	—	12	—	pF	f=1.0MHz

**Source-Drain Ratings and Characteristics**

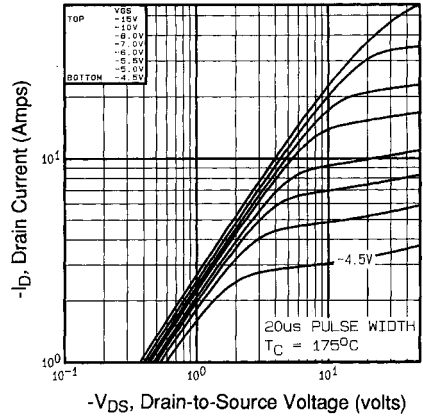
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	-7.7	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	-31		
V <sub>SD</sub>	Diode Forward Voltage	—	—	-6.3	V	T <sub>J</sub> =25°C, I <sub>S</sub> =-7.7A, V <sub>GS</sub> =0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	120	240	ns	T <sub>J</sub> =25°C, I <sub>F</sub> =-12A
Q <sub>rr</sub>	Reverse Recovery Charge	—	0.46	0.92	μC	di/dt=100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

**Notes:**

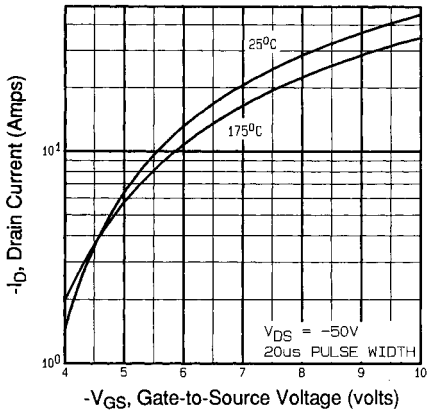
- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② V<sub>DD</sub>=-25V, starting T<sub>J</sub>=25°C, L=9.6mH R<sub>G</sub>=25Ω, I<sub>AS</sub>=-7.7A (See Figure 12)
- ③ I<sub>SD</sub>≤-7.7A, di/dt≤140A/μs, V<sub>DD</sub>≤V<sub>(BR)DSS</sub>, T<sub>J</sub>≤175°C
- ④ Pulse width ≤ 300 μs; duty cycle ≤2%
- ⑤ t=60s, f=60Hz



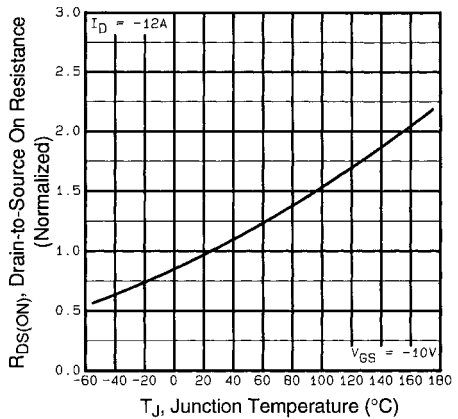
**Fig 1.** Typical Output Characteristics,  
 $T_C=25^\circ\text{C}$



**Fig 2.** Typical Output Characteristics,  
 $T_C=175^\circ\text{C}$

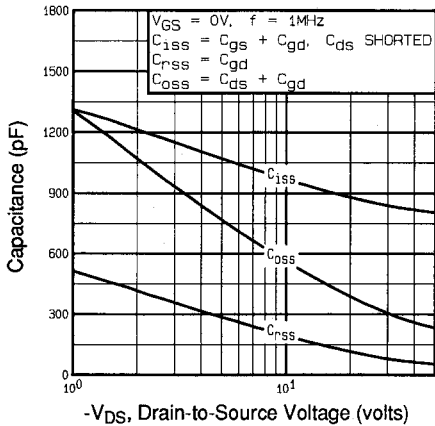


**Fig 3.** Typical Transfer Characteristics

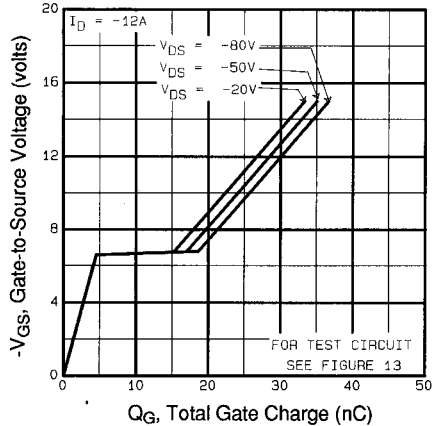


**Fig 4.** Normalized On-Resistance  
Vs. Temperature

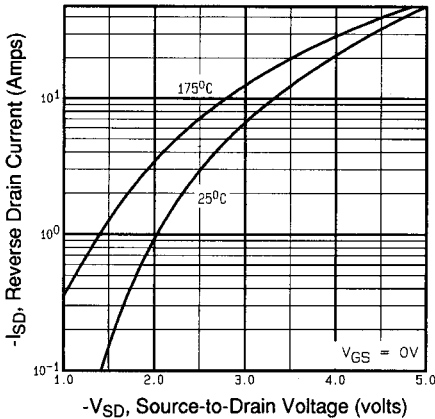
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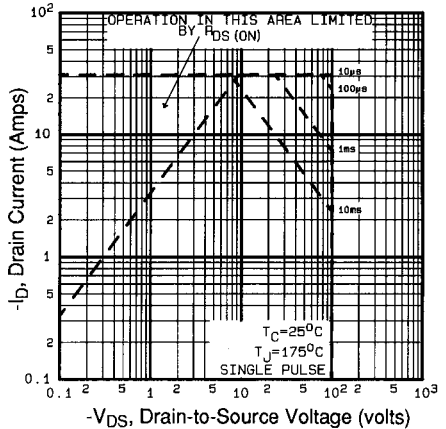
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



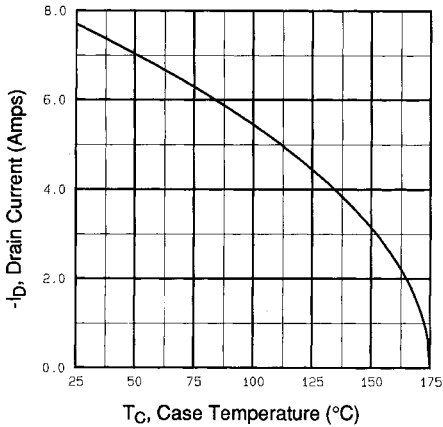
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



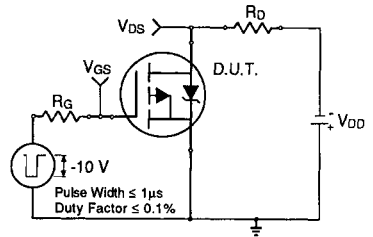
**Fig 7.** Typical Source-Drain Diode Forward Voltage



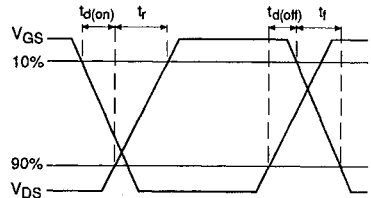
**Fig 8.** Maximum Safe Operating Area



**Fig 9.** Maximum Drain Current Vs. Case Temperature

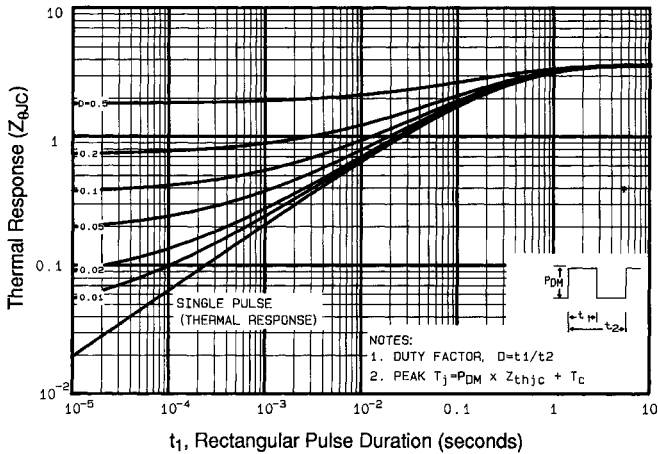


**Fig 10a.** Switching Time Test Circuit

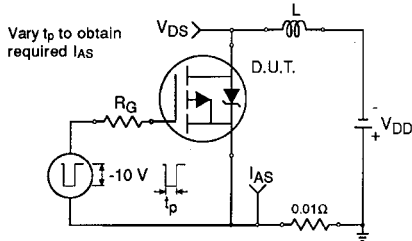


**Fig 10b.** Switching Time Waveforms

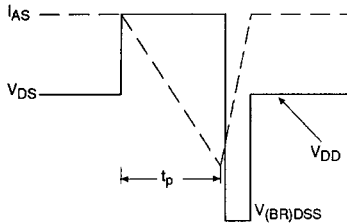
DATA SHEETS



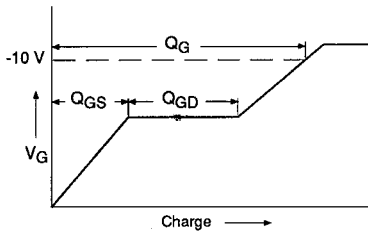
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



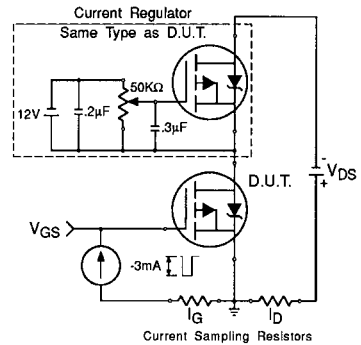
**Fig 12a.** Unclamped Inductive Test Circuit



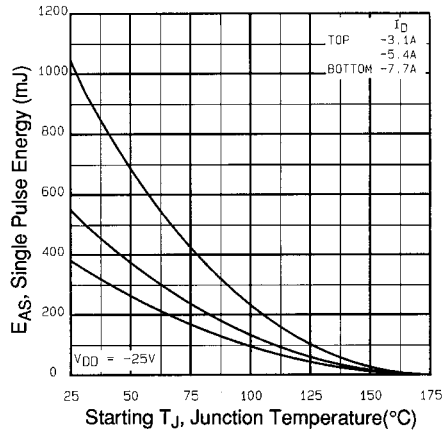
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

**Appendix A:** Figure 14, Peak Diode Recovery  $dv/dt$  Test Circuit – See page 1506

**Appendix B:** Package Outline Mechanical Drawing – See page 1510

**Appendix C:** Part Marking Information – See page 1517

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